Performance Review of Integrated CMOS VCO Circuits for Wireless Communications

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***Abstract*—This paper reviews monolithically integrated CMOS Voltage Controlled Oscillators (VCO) for wireless communications. The key challenges in VCO development include: design of a high Q tank on a substrate tailored for CMOS, multiband operation using a single VCO, enhanced manufacturability using digital frequency tuning, and optimization of the overall VCO topology for low power operation. Recent developments in each of these areas are examined and a comparison of various VCO topologies versus Figure of Merit (FOM) is presented.**

I. INTRODUCTION

CMOS LC monolithic integrated VCO's continue to be a subject of increased research [1-12]. Much of the published work focuses on designing a high Q tank to achieve a given phase noise target with minimum power. However, from an overall systems perspective, other issues such as tuning range, VCO gain (MHz/volt) and the ability to switch bands using only one VCO are equally important. Most modern cellular phones are expected to operate over several frequency bands. Hence, an ability to switch bands without significant degradation in VCO performance is an important design goal. The objective of this paper is to review the fundamental aspects of high performance CMOS VCO design as well as address recent developments in areas, such as digital frequency tuning of VCO's for multi-band operation and enhanced manufacturability.

VCO design issues can be captured with a modified Leeson's formula [1, 2, 12], which states

$$S_{SSB}(\delta\omega)=\frac{2FKT}{P_s}\left\{\left(1+\left(\frac{1}{2Q}\frac{\omega_c}{\delta\omega}\right)^2\right)\left(1+\frac{\omega_{1/f^3}}{\delta\omega}\right)+\frac{\pi^2}{2}\left(\frac{K_V V_m}{\delta\omega}\right)^2\right\} \quad (1)$$

where S_{SSB} is the single sideband phase noise, Q is the loaded quality factor of the tank, P_S is the average signal power, F is the device noise factor, ω_C is the oscillation frequency, $\delta\omega$ is the offset frequency, ω_{1/f^3} is the corner frequency between ω_{1/f^2} and ω_{1/f^3} portion of the phase noise spectrum, Kv is the gain of the VCO in Hz/V and Vm is the total amplitude of low frequency noise coming from sources, such as tune line.

From the above equation it is clear that VCO phase noise decreases quadratically with the quality factor of the tank. Hence, design of a high quality tank is the most important aspect of VCO development. Historically, designers have focused on integrated inductor design since it is difficult to reduce loss in a Si substrate tailored for CMOS, which leads to lower Q. However, with the recent improvements in the quality factor of integrated inductors it has become critical to achieve high quality factor (Q) varactors. The quality factor of an LC tank can be written as:

$$\frac{1}{Q}=\frac{1}{Q_L}+\frac{1}{Q_C} \quad (2)$$

where Q_L and Q_C are quality factors of inductor and capacitor. To underscore the importance of varactor design, we can look at an example scenario. If we can achieve a quality factor of 20 for the integrated inductors, we would still need a varactor with a Q of 60 to make a tank with an unloaded Q of 15. Achieving a high quality factor varactor at 4-5GHz frequency range is certainly challenging. Hence, the design and layout of varactors have become very critical with improvement in integrated inductor design.

The second term in the phase noise equation describes contribution of 1/f noise from devices, which appears as $1/f^3$ noise in the VCO phase noise spectrum [1]. Choice of VCO topology plays a key role in minimizing the contribution of 1/f noise. Topology and biasing are important determinants of VCO performance, particularly in low power arena where phase noise per mW of dissipated power is the performance metric.

The last term in the phase noise equation emphasizes the need for achieving a low VCO gain to reduce phase noise from low frequency noise sources. Low frequency noise could come from the tune line and may dominate phase noise if the VCO gain is high. Designers have to be particularly careful about this when designing digitally tuned VCO's for multi band operation.

VCO design can be broadly divided into three tasks: choice and optimization of topology, design of tank and

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design of tuning circuits/approaches to achieve multi band operation. In this paper, we review developments in each of these areas as well as performances of some recently published VCO's.

II. VCO CORE TOPOLOGIES

MOS VCO topologies (Fig. 1) can be classified into two categories: 1) nMOS only core and 2) Complementary core (CMOS) which uses both nMOS and pMOS MOSFET's in a cross-coupled fashion. Each of these topologies can be further modified by adding a tail current source, which controls whether the devices operate in the so called *voltage limited* or *current limited* regime [1]. For the same current consumption, the CMOS version exhibits better phase noise than the nMOS only version [1]. This superiority is due to the fact that CMOS structures provide higher transconductance for a given bias current, which results in faster switching of the cross-coupled differential pair. CMOS topologies have better rise/fall time symmetry, which tends to reduce the $1/f^3$ corner frequency [1]. One disadvantage of this topology is that the maximum signal swing is limited to the supply voltage. In situations where the supply voltage is low, nMOS only structures could be an option since they can provide voltage swings greater than the supply voltage but at the expense of increased current drain and reduced efficiency. Large voltage swings above supply voltage could be a reliability issue.

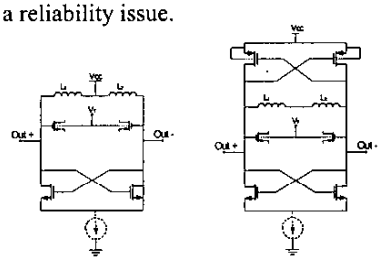

Fig. 1. Differential VCO topologies with nMOS & CMOS core and optional current source.

Addition of tail current to the VCO core has its trade-offs. The tail current source limits the voltage swing across the tank and adds noise to the overall VCO phase noise. However, the advantage of a tail current is that it sets the bias of the differential pair making it less immune to supply voltage variation. A current source also provides a high impedance to the tank (only to even harmonics) to reduce loading of the tank by the MOSFET's. In summary, the choices are: a) No tail current with a reliable voltage regulator so that the impact of supply voltage fluctuation on VCO phase noise is reduced; or 2) Current source biasing with filters to reduce noise contribution from the current source to the overall phase noise of the VCO [3].

Another topology that is gaining interest is the quadrature VCO [4]. These circuits consist of two cross-coupled VCOs and are used to generate signals in quadrature. This topology eliminates the quadrature generation circuit and reduces the overall current consumption. However, this topology requires a larger die area because it includes two tank circuits. There is also the potential of LO leakage at the receive frequency.

III. INTEGRATED PASSIVES

The key driver of integrated VCO performance is the quality factor of on-chip inductors and capacitors including varactors. Approaches to generate high Q inductors are: a) reduce resistance of the coil, b) make the dielectric layer underneath the coil as thick as possible, c) reduce substrate loss, and d) connect the inductor differentially to reduce capacitance to ground. Reduction of series resistance has the biggest impact on inductor Q. A thick top metal layer is necessary to reduce series resistance of coils. Most of the CMOS technologies offer a thick Al top metal layer of thickness 3-4 um for inductor design. In Motorola's 0.18μm BiCMOS technology, a 10μm thick electroplated copper with sheet resistance of 2mOhm/sq is used for inductor design.

Another important technique to improve inductor Q is to connect the inductor differentially. An improvement of Q factor by 30% was observed by exciting the coil differentially. Figure 2 shows the layout and measured Q of a 2nH inductor that was manufactured using 10μm copper layer. In this case the inductor had maximum differential Q of 30 at a frequency of 5.5GHz.

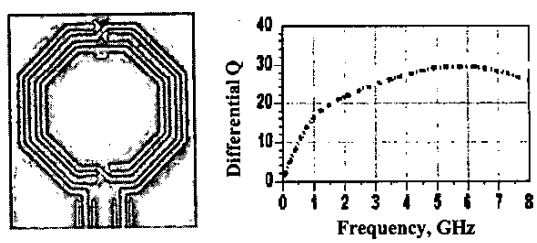

Fig. 2. Differential inductor layout and measured Q.

With the improvements in integrated inductor Q, the varactor quality factor has become increasingly important in determining the overall tank quality factor. Key issues in varactor design are: a) reduction of series resistance to improve Q, and b) Improvement of C_{MAX}/C_{MIN} ratio to increase tuning range. C_{MAX} and C_{MIN} are the maximum

and minimum value of varactor capacitance as a function of the tuning voltage. MOS varactors are preferable since they can be optimized to give higher Q and tuning range compared to diode varactors. However, one disadvantage is their steep capacitance variation with tuning voltage, which might lead to the undesirable effect of higher VCO gain.

Classical concept of differential circuit can be applied to the design of varactors, which leads to reduced series resistance [11]. Figure 3 shows an example differential MOS varactor. In the case of differential varactors, the n-well contact between MOS gates is omitted since a ground plane exists between the two MOS gates because of the differential signal between plus and minus terminals. Removal of n-well contact leads to more compact layout and reduced n-well resistance, which in turn improves varactors' quality factor (Q).

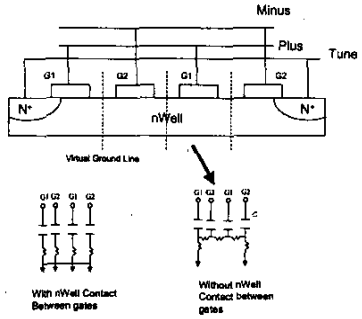

Fig. 3. Differential MOS varactor to reduce n-well resistance [11].

III. PERFORMANCE TRENDS

Numerous papers describing CMOS VCO's have been published in recent years [3-10]. To compare the performance of various VCO's, a commonly accepted approach is to use a figure of merit (FOM), which is given as

$$FOM = S_{SSB}\left(\frac{\delta\omega}{\omega_c}\right)^2 P_{VCO}/mW \qquad (3)$$

where P_{vco} is the total power consumed by the VCO. Note that the total power, P_{VCO}, consumed by the VCO is more than P_S in equation (1) and includes losses in the circuit. A closer look at the FOM equation and equation (1) reveals that FOM is essentially a normalized metric of device noise factor F over Q^2.

A review of VCO's published in recent years shows that the improvement in performance has primarily come from two sources: a) topological enhancements; and b) improvements in the quality of integrated inductors and MOS varactors. Figure 4 shows a plot of FOM versus various topologies adopted in CMOS VCO's. The simplest topology, which is CMOS without any current

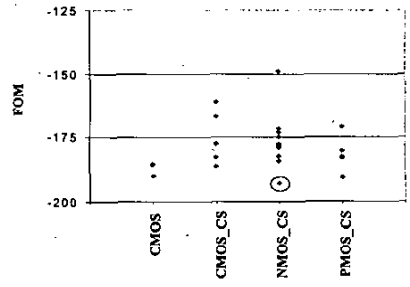

Fig. 4. FOM vs. VCO topologies. CMOS_CS refers to CMOS core with current source. nMOS and pMOS are with nMOS/pMOS core. Circled data is nMOS_CS with a noise filter [3].

source, shows excellent performance. Review of published data shows that the addition of a current source is advisable only if it is accompanied by a filter to reduce noise contribution from the current source. The circled data point in Fig. 4 is one such example [3]. Figure 4 also shows that the use of pMOS, which has lower flicker noise than nMOS, doesn't necessarily lead to better FOM.

Improvement from the quality of integrated inductors is critical. Our review of published data shows that one of the best FOM was obtained through use of bondwire inductors [7]. The downside is higher manufacturing tolerance.

IV. SYSTEMS INTEGRATION ISSUES

Integration of a VCO into a receiver/transmitter IC requires careful consideration of VCO gain which is not captured in the FOM equation of the VCO. VCO is part of a Phased Locked Loop. It is essential to tightly control the gain of the VCO for optimal PLL design. A closed loop transfer function of a PLL is described by the following equation,

$$H(s) = \frac{NK_v K_\phi F(s)}{sN + K_v K_\phi F(s)} \qquad (4)$$

Where K_V is the VCO gain (radian/Volts), $K\phi$ is the Phase detector gain (Volts/radian or Amps/ radian), F(s) is the loop filter transfer function, and N is the divider ratio. The PLL response is optimized for both reference spur rejection and lock-time. The poles and zeros, for the given order of a PLL, are placed to get maximum spur rejection without compromising lock-time requirements of the VCO. Since the closed loop response is a function of K_V,

variation in K_V affects lock-time and stability of the loop. A maximum 2:1 Kv is usually necessary, with 10% loop filter's passive components variations, to guarantee Six-Sigma PLL design.

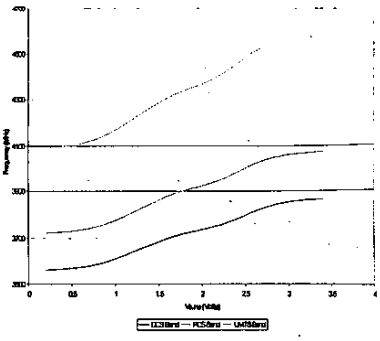

Fig. 5. Measured tri-band VCO frequency versus tuning voltage. Single VCO covers all 3GPP (2100, 1900, 1800 MHz) bands.

Lower VCO gain is also desirable from the point of view of phase noise as evident from equation (1). Higher VCO gain makes the radio board design difficult since any noise in the tune line gets converted into additional phase noise.

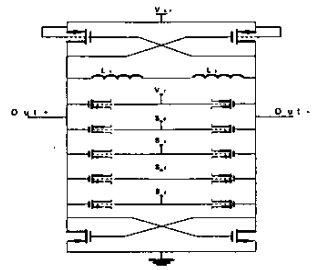

Fig. 6. 4-bit digitally -tuned VCO. Each VCO sector can be selected based on an algorithm and fine tuning is done within a sector.

A lower VCO gain, on the other hand, restricts the use of the VCO for more than one band since the tuning range is reduced. However, advanced cellular handsets require multi-band operation with single VCO to reduce die area of the IC's. A compromise between the requirements of lower VCO gain and multi-band operation with a single VCO is achieved using discrete frequency tuning and auto-calibration methods [3, 5]. The simplest form of coarse digital tuning can be done by using a set of fixed binary weighted capacitors to move the VCO center frequency in discrete sub-bands. Fine frequency tuning within a closed PLL loop is done only within a band. Another approach is to use proportionally sized digitally controlled MOS varactors to switch bands. Figure 5 shows a VCO which can be digitally tuned to cover UMTS, PCS and DCS bands by using two bits. Figure 6 shows an example implementation where the VCO tuning range has been divided into 2^4 discrete bands for coarse digital tuning with 4 bits.

V. CONCLUSION

A review of current integrated VCO circuits has been presented. Current published data indicates that CMOS VCO's are suitable to meet most wireless communication systems' needs. However, challenges in designing CMOS integrated VCO's remain. The difficulties are created by the fact that future VCO's will be realized in digital technologies with lower supply/breakdown voltages. Lower supply voltage will limit the output voltage swing, which in turn, will degrade phase noise and reduce tuning range. Continued improvement in integrated inductor/varactor quality factor coupled with circuit level innovation will be required to design VCO's in a low voltage CMOS technology to meet cellular wireless specifications.

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